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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,793	10/29/2003	Katherine L. Saenger	20140-00312-US1	6060

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EXAMINER	
SARKAR, ASOK K	
ART UNIT	**PAPER NUMBER**
2891	

DATE MAILED: 04/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/694,793	SAENGER ET AL.	
	Examiner	Art Unit	
	Asok K. Sarkar	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) *23-39* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/29/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I claims, 1 – 22 in the reply filed on March 01, 2005 is acknowledged.

2. Claims 23 – 39 were withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Group II claims, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on March 01, 2005.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 4, 9 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Lopatin, US 6,440,830.

Regarding claim 1, Lopatin teaches a method for making a metal gate for a field effect transistor, said metal gate comprising plated material, said method comprising:

- selecting a substrate 100 having a top surface and a recessed region 202 extending below said top surface, said recessed region defining the position and dimensions desired for said metal gate (see Fig. 2);
- conformally depositing a conductive seed layer 304 on said substrate;
- electroplating a filler gate metal 306 on said conductive seed layer to 304 and

overfill said recessed region (see Fig. 3); and

- removing at least a portion of said filler gate metal and said conductive seed layer to expose at least a portion of said top surface of said substrate (see Fig. 4)

in descriptions between column 3, line 35 and column 4, line 52.

Regarding claim 2, Lopatin teaches removing the filler gate material and the seed layer to expose a portion of the top surface of the substrate by polishing in column 4, lines 45 – 52.

Regarding claim 4, Lopatin teaches depositing a conductive cladding layer 302 with reference to Fig. 3 in column 4, lines 8 – 13.

Regarding claims 9 and 10, Lopatin teaches cladding layers of conductive metal nitrides that are doped with nitrogen in column 4, lines 16 – 22.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lopatin, US 6,440,830 in view of Seibel, US 6,777,317.

Lopatin fails to teach the dimension of the recessed region.

Seibel teaches that the present semiconductor technology requires submicron gate dimensions for MOSFET productions in column 1, lines 18 – 26.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention that the recessed region in Lopatin's gate will be less than 1 micron wide and less than 1 micron deep for the benefit of producing submicron size gates as taught by Seibel in column 1, lines 18 – 26 for the production of present day MOSFETs.

9. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lopatin, US 6,440,830 in view of Andricacos, US 6,188,120.

Lopatin fails to teach a through-mask electroplating process prior to plating the filler gate material.

Andricacos teaches a through-mask electroplating process for the benefit of selective electroplating in defined areas in column 1, lines 1 – 30.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Lopatin, and use a through-mask electroplating process for the benefit of selective electroplating in defined areas as taught by Andricacos in column 1, lines 1 – 30.

10. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lopatin, US 6,440,830 in view of Seibel, US 6,777,317 and Horii, US 6, 255,187.

Lopatin teaches the thickness of the cladding layer in column 4, lines 20 – 23, but fails to teach the dimension of the recessed region and the thickness of the seed layer.

Seibel teaches that the present semiconductor technology requires submicron gate dimensions of 100 – 250 nm for MOSFET productions in column 1, lines 18 – 26.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention that the recessed region in Lopatin's gate will be in the range of 20 – 500 nm wide and 20 – 300 nm deep for the benefit of producing submicron size gates as taught by Seibel in column 1, lines 18 – 26 for the production of present day MOSFETs.

Horii teaches that for electroplating various noble metals, seed layers of different thickness are needed for the benefit of forming a robust filler material within a cavity under descriptions in columns 5 and 6.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention that the recessed region in Lopatin's gate will have a to judiciously

adjust and control these thickness for the seed layer and the cladding layers during the electroplating process of the filler metal within a narrow recess regions of the gate through routine experimentation and optimization to achieve optimum benefits (see MPEP 2144.05) and it would not yield any unexpected results.

Note that the specification contains no disclosure of either the critical nature of the claimed processes or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen methods or upon another variable recited in a claim, the Applicant must show that the chosen methods or variables are critical (*Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir., 1990)). See also *In re Aller, Lacey and Hall* (10 USPQ 233 – 237).

11. Claims 7, 8 and 11 – 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lopatin, US 6,440,830 in view of Horii, US 6, 255,187.

Regarding claims 7, 8 and 17, Lopatin teaches the filler metal as Cu and teaches that other high conductivity metals can be used in place of Cu, but fails to teach seed layer containing metals other than Cu.

Horii teaches that when the filler metal is a platinum group metal (see for example column 7, lines 12 – 30), the seed layers can be formed of various metals either by itself or doped with nitride or oxide for the benefit of forming improved contacts in column 6, lines 8 – 20.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention that when the recessed region in Lopatin's gate is filled with other metals such as from that of the platinum group, the seed layers can be formed of

various metals either by itself or doped with oxide for the benefit of forming improved contacts as taught by Horii in column 3, lines 21 – 31.

Regarding claims 11 – 16, Lopatin teaches conductive cladding layers of metal or metal nitride of Ti and Ta, but fails to teach filler gate materials other than Cu.

Horii teaches that when the filler metal is a platinum group metal such as Pt, Ir, Rh and Ru (see for example column 7, lines 12 – 30), the cladding layers can be formed of various metals and alloys for the benefit of forming improved contacts in between column 5, line 52 and column 6, line 3.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention that when the recessed region in Lopatin's gate is filled with other metals such as from that of the platinum group including Ru, the cladding layer can be formed of various metals and alloys for the benefit of forming improved contacts as taught by Horii in column 3, lines 21 – 31.

12. Claims18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gao, US 6,873,048 in view of Doczy, US 2005/0037557 and Lopatin, US 6,440,830.

Regarding claim 18, Gao teaches a method for making a metal gate for a n-FET and a P-FET, said method comprising:

- selecting a substrate having a top surface and at least two recessed regions extending below said top surface, said recessed regions defining at least one n-FET gate and at least one p-FET gate with reference to Fig. 1;

- blanket depositing a seed layer 200 with an n-FET work function on said substrate (see Fig. 2);
- masking off the at least one n-FET gate with resist (see Fig. 6, the position of the FET can be switched);
- selectively depositing a layer 300 allowing for a p-FET work function on the at least one p-FET gate (see Fig. 6, the position of the FET can be switched);
- removing the resist over the at least one n-FET gate (see Fig. 7, the position of the FET can be switched) in descriptions for Figures 1 – 6 under column 3 and also various other approaches as taught by Gao for switching the metals for the two FET regions to optimize the metal work functions for the two gates.

Gao fails to teach 1) selectively plating a layer allowing for a p-FET work function on the at least one p-FET gate and 2) annealing the metal layers deposited over the at least one p-FET gate to form an annealed layer with a p-FET work function.

Regarding element 1, Doczy teaches that conductive layers for the gate electrode can be deposited by electroplating for the benefit of selective deposition in paragraph 39.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Gao and deposit the p-FET work function metal by electroplating for the benefit of applying a selective deposition technique as taught by Doczy in paragraph 39.

Regarding element 2) Lopatin teaches that an annealing step should be performed after electrodeposition of a metal for the benefit of forming a reliable

electrical contact between the various layers deposited within the gate in column 4, lines 39 – 44.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Gao in view of Doczy and perform an annealing step after the electrodeposition of the metal for the benefit of forming a reliable electrical contact between the seed layer and the electrodeposited layer within the gate as taught by Lopatin in column 4, lines 39 – 44.

Regarding claim 19, Gao in view of Doczy and Lopatin, teaches the steps of filling the recessed layer with filler metal by electroplating to complete the gate formation and then conventional CMP process (see column 3, lines 42 – 50) to remove the excess seed layer and the filler metal with reference to Fig. 9.

13. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gao, US 6,873,048 in view of Doczy, US 2005/0037557 and Lopatin, US 6,440,830 as applied to claim 19 above, and further in view of Seibel, US 6,777,317.

The limitations of this claim have been described earlier in rejecting claim 3.

14. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gao, US 6,873,048 in view of Doczy, US 2005/0037557 and Lopatin, US 6,440,830 as applied to claim 19 above, and further in view of Forbes, US 2004/0036129.

Gao in view of Doczy and Lopatin fails to teach using Ru-Ta alloy for n-FET work function and using Ru for the p-FET work function.

Forbes teaches that tuned Ru-Ta alloy is excellent for n-FET gate electrode work function and Ru is excellent for p-FET gate electrode work function in paragraph 5.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Gao in view of Doczy and Lopatin and use Ru-Ta alloy for n-FET work function and use Ru for the p-FET work function since these two materials are excellent for n-FET gate electrode work function and for p-FET gate electrode work function respectively as taught by Forbes in paragraph 5.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on 571 272 1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

16. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Asok Kumar Sarkar

Asok K. Sarkar
April 11, 2005

Primary Examiner